WM5621L

Production Data
Jan. 1997 Rev. 1.0

Low-power Quadruple 8-Bit DAC

Description

WM5621L is a quadruple 8-bit digital to analogue converter (DAC) with buffered reference inputs (high impedance). The DAC produces an output voltage that ranges between either one or two times the reference voltage and GND. The DAC is monotonic. The device operates from a single supply in the range 2.7V to 5.5V. A power-on reset function is incorporated to provide repeatable start-up conditions. A global hardware shut-down terminal and the capacity to shut-down each individual DAC with software are provided to minimize power consumption.

WM5621L interfaces to all popular microcontrollers and microprocessors via a three wire serial interface with CMOS compatible, schmitt trigger, digital inputs. Alternatively a two wire serial interface can be activated. An 11-bit command word consists of eight bits of data, two DAC select bits and a range bit for selection between the times one or times two output range. The DACregisters are double buffered which allows a complete set of new values to be written to the device, and then under control of HWACT, all of the DAC outputs are simultaneously updated.

Ideal in space critical applications WM5621L is available in small outline and DIP packages and is characterized for operation from -25ºC to 85ºC.

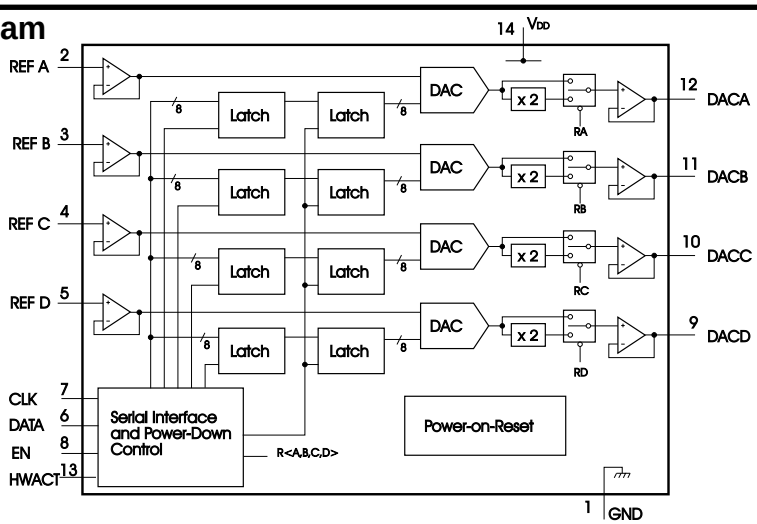
Features

- **Individual (or all) DAC's can be powered-down**
- **One low-power 8-bit voltage output DAC**
- **Three 8-bit voltage output DACs**
- **Fast serial interface (1 MHz max)**
- **Simple 2 or 3 wire interface**
- **Programmable for 1 or 2 times output range**
- **High impedance reference inputs for each DAC**
- **Simultaneous update facility**
- **Extended temperature range (-25ºC to 85ºC)**
- **Single supply operation, range 2.7 V to 5.5 V**
- **0 to 4 V output (x2 output range) at 5 V V_{DD}**
- **0 to 2.5 V output (x2 output range) at 3 V V_{DD}**
- **Low power specification:**
  - **All DACs on : 3.6 mW at 3.6 V typ**
  - **: 6 mW at 5 V typ**
  - **Low power DAC : 0.54 mW at 3.6V typ**
  - **All DAC's shutdown : 0.18 mW at 3.6V typ**
- **Guaranteed monotonic output**

Applications

- **Mobile Communications**
- **Programmable d.c. voltage sources**
- **Digitally controlled attenuator/amplifier**
- **Signal synthesis**
- **Automatic test equipment**

Block Diagram



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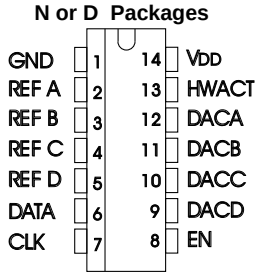
Pin Configuration

Top View
N or D Packages



Ordering Information

DEVICE	TEMP. RANGE	PACKAGE
WM5621LED	-25°C to 85°C	14 pin plastic SO
WM5621LEN	-25°C to 85°C	14 pin DIP

Absolute Maximum Ratings (note 1)

Supply Voltage (V_{DD} - GND) . . . . . +7V
Digital Inputs . . . . . GND - 0.3 V, V_{DD} + 0.3 V
Reference inputs . . . . . GND - 0.3 V, V_{DD} + 0.3 V

Operating temperature range, T_A . . . . . -25°C to +85°C
Storage Temperature . . . . . -50°C to +150°C
Lead Temperature (soldering, 10 sec) . . . . . +260°C

Recommended Operating Conditions

	MIN	NOMINAL	MAX	UNIT
Supply Voltage	2.7	3.3	5.5	V
Reference input range	GND		V_{DD} - 1.5	V
DAC output load resistance to GND	10			kΩ
High level digital input voltage	0.8 V_{DD}			V
Low level digital input voltage			0.2 V_{DD}	V
Clock frequency			1	MHz
Operating free-air temperature, T_A	-25		85	°C

Electrical Characteristics

V_{DD} = 3 V to 3.6V, GND = 0 V, V_{REF} = 1.25 V, R_L = 10 kΩ, C_L = 100 pF, x1 gain output range, T_A = full range unless otherwise stated.

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage	VDD	see note 2	2.7	3.3	5.5	V
High level digital input voltage	VIH		0.8 VDD			V
Low level digital input voltage	VIL				0.2 VDD	V
Reference voltage, VREF [A|B|C|D]		x1 gain	GND		VDD-1.5	V
Load resistance	RL		10			kΩ
Data input setup time	tSD		50			ns
Data input hold time	tHD		50			ns
CLK ↓ to EN ↓	tEN	see note 3	100			ns
EN ↑ to CLK ↓	tLC	see note 3	100			ns
CLK period high	cph	see note 3	400			ns
EN low time	tenl		200			ns
Clock frequency	fCLK				1.0	MHz
Operating free-air temperature	TA		-25		85	°C

Electrical Characteristics (continued)

V_{DD} = 3 V to 3.6V, GND = 0 V, V_{REF} = 1.25 V, R_L = 10 kΩ, C_L = 100 pF, x1 gain output range, T_A = full range unless otherwise stated.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Max. full-scale output voltage	Vomax	Vref=1.5V, open cct. output ,x2 gain	VDD-100	2		mV
High level input current	IIH	VI = VDD			± 10	µA
Low level input current	IIL	VI = 0V			± 10	µA
Output sink current DACA	Io (sink)	at DAC code 0	5			µA
Output sink current DACB	Io (sink)	at DAC code 0	20			µA
Output Source Current	Io (source)	Each DAC output, at DAC code 255	1			mA
Input capacitance	CI			15		pF
Reference input capacitance		A, B, C, D inputs		15		pF
Supply current	IDD	VDD = 3.6V		1	1.5	mA
		VDD = 5.0V		1	1.5	mA
Supply current One low power DAC Active	IDAC	VDD = 3.6V (Note 4)		150	250	µA
Supply Current ALL DACs Shutdown	Iddsd	VDD = 3.6V (see note 4)		50	100	µA
Reference input current	IREF	A, B, C, D inputs			± 10	µA
Integral Nonlinearity	INL	VREF = 1.25V, Range x2. (note 5,13)			± 1.0	LSB
Differential Nonlinearity	DNL	VREF = 1.25V, Range x2. (note 6,13)		± 0.1	± 0.9	LSB
Zero scale error	ZCE	VREF = 1.25V,Range x2. (note 7)	0		30	mV
Zero scale error temperature coefficient		VREF = 1.25V,Input code = 00 Hex (note 8)		10		µV/^{O}C
Zero scale error supply rejection				2		mV/V
Full scale error	FSE	Range x 2. (note 9)			± 60	mV
Full scale error temperature coefficient		VREF = 1.25V,Range x2. (note 10)		± 25		µV/^{O}C
Full scale error supply rejection				2		mV/V
Feedback resistor network resistance				168		kΩ

Notes:

1. Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating range limits are given under Recommended Operating Conditions. Guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.
2. The device operates over the supply voltage range of 2.7V to 5.5V. Over this voltage range the device responds correctly to data input by changing the voltage output but conversion accuracy is not specified over this extended range.

Electrical Characteristics

V_{DD} = 3 V to 3.6V, GND = 0 V, V_{REF} = 1.25 V, R_L = 10 kΩ, C_L = 100 pF, x1 gain output range, T_A = full range unless otherwise stated.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate rising DACA				0.8		V/µS
Output slew rate falling DACA				0.5		V/µS
Output slew rate DACB,C,D				1		V/µS
Output settling time rising DACA		To 1/2 LSB, VDD=3V		20		µS
Output settling time falling DACA		To 1/2 LSB, VDD=3V		75		µS
Output settling time rising DACB,C,D		To 1/2 LSB, VDD=3V		10		µS
Output settling time falling DACB,C,D		To 1/2 LSB, VDD=3V		75		µS
Output settling time HWACT or ACT↑ to output volts DACA (note 14)		To 1/2 LSB, VDD=3V		40	120*	µS
Output settling time HWACT or ACT↑ to output volts DACB,C,D (note 14)		To 1/2 LSB, VDD=3V		25	75*	µS
Large signal Bandwidth		Measured at -3dB point		100		KHz
Digital crosstalk		CLK=1MHz sq. wave measured at DACA-DACD		-50		dB
Reference feedthrough		A,B,C,D inputs (note 15)		-60		dB
Channel-to-channel isolation		A,B,C,D inputs (note 16)		-60		dB
Channel-to-channel isolation when in shutdown		A,B,C,D inputs		-40		dB
Reference bandwidth DACA		note 17		20		kHz
Reference bandwidth DACB,C,D		note 17		100		kHz

Notes:

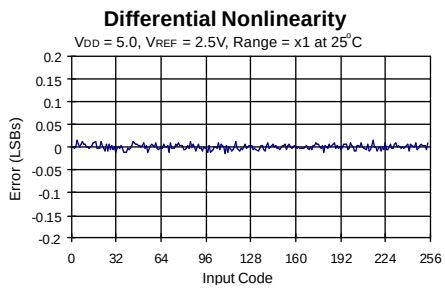
3. This is tested by design but is not production tested.
4. This is measured with no load (open circuit output), Vref = 1.25V, range = x2.
5. Integral Nonlinearity (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full-scale errors).
6. Differential Nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. A guarantee of monotonicity means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
7. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
8. Zero scale error temperature coefficient is given by: $ZCETC = (ZCE(T_{max}) - ZCE(T_{min}))/V_{REF} \times 10^6/(T_{max} - T_{min})$
9. Full-Scale error is the deviation from the ideal full-scale output (Vref - 1LSB) with an output load of 10kΩ.
10. Full-Scale Temperature Coefficient is given by: $FSETC = (FSE(T_{max}) - FSE(T_{min}))/V_{REF} \times 10^6/(T_{max} - T_{min})$
11. Zero-code Error Rejection Ratio (ZCE-RR) is measured by varying the V_{DD} voltage, from 4.75 to 5.25 V d.c., and measuring the proportion of this signal imposed on the zero-code output voltage.

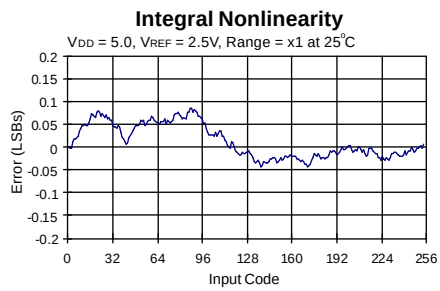
Electrical Characteristics (continued)

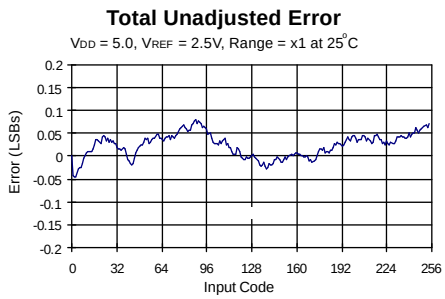
12. Full Scale Error Rejection Ratio (FSE-RR) is measured by varying the V_{DD} voltage, from 4.75 to 5.25 V d.c., and measuring the proportion of this signal imposed on the full-scale output voltage.
13. Linearity is only specified for DAC codes 1 through 255.
14. The ACT bit is latched on falling edge of EN.
15. Reference feedthrough is measured at any DAC output with an input code = 00 hex with a Vref input = 1Vdc + 1 Vpp at 10kHz.
16. Channel-to-channel isolation is measured by setting the input code of one DAC to FF hex and the code of all other DACs to 00 hex with Vref input = 1Vdc + 1 Vpp at 10kHz.
17. Reference bandwidth is the -3dB bandwidth with an ideal input at Vref = 1.25 Vdc + 2 Vpp and with a digital input code of full-scale (range set to x1 and Vdd = 5V)

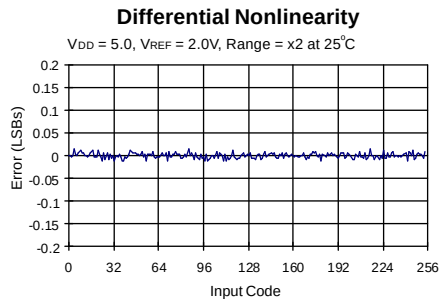
Typical Performance Characteristics

Typical DNL, INL and TUE at VDD = 5 V



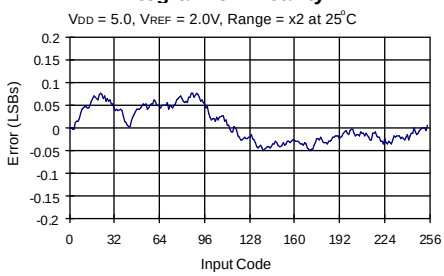




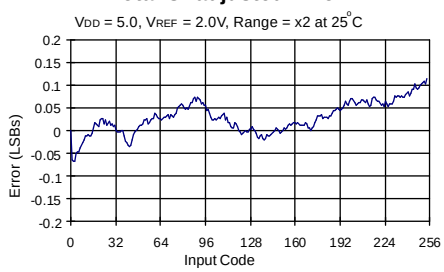


Typical Performance Characteristics (continued)

Integral Nonlinearity

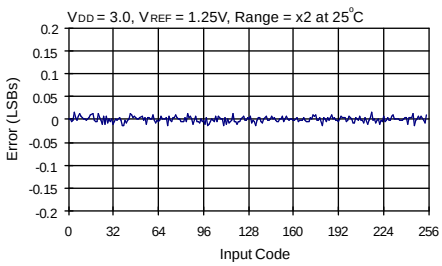


Total Unadjusted Error

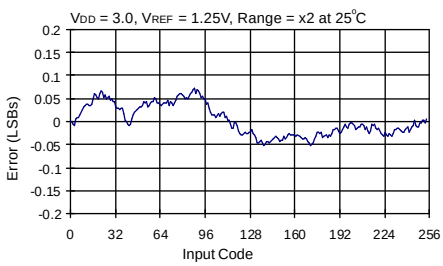


Typical DNL, INL and TUE at VDD = 3 V

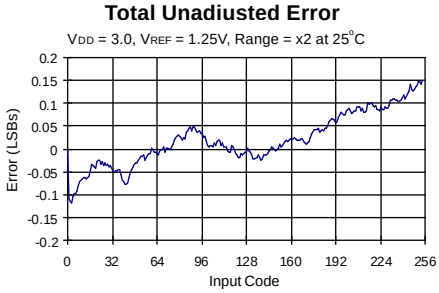
Differential Nonlinearity



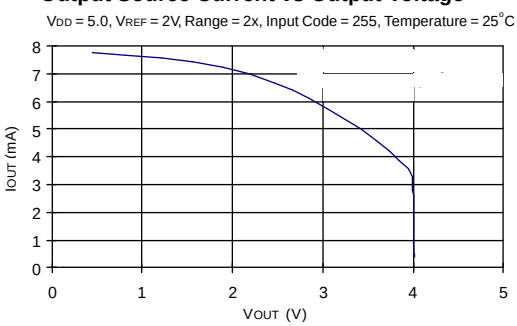
Integral Nonlinearity



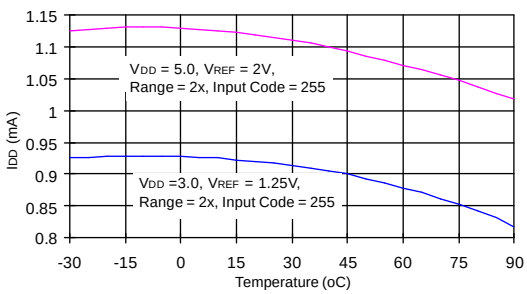
Total Unadiusted Error



Output Source Current vs Output Voltage

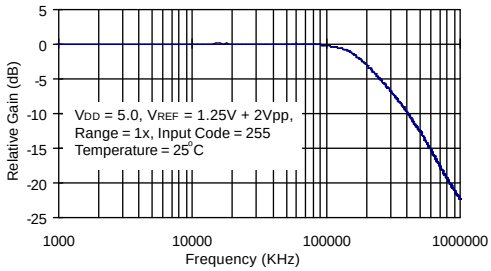


Supply Current v Temperature

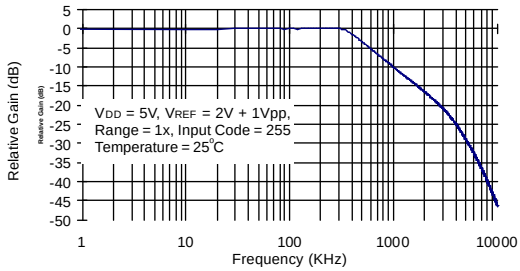


Typical Performance Characteristics (continued)

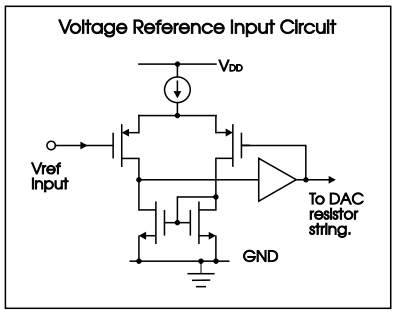
Large Signal Frequency Response

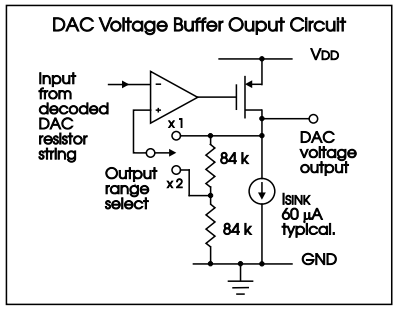


Small Signal Frequency Response



Input and Output Circuits





Pin Descriptions

Pin	Name	Type	Function
1	GND	Supply	Ground return and reference terminal
2	REFA	Analogue input	Reference voltage input to DACA
3	REFB	Analogue input	Reference voltage input to DACB
4	REFC	Analogue input	Reference voltage input to DACC
5	REFD	Analogue input	Reference voltage input to DACD
6	DATA	Digital input	Serial interface data
7	CLK	Digital input	Serial interface clock, negative edge sensitive
8	EN	Digital input	Input Enable
9	DACD	Analogue output	DAC D output
10	DACC	Analogue output	DAC C output
11	DACB	Analogue output	DAC B output
12	DACA	Analogue output	DAC A output
13	HWACT	Digital input	Hardware activate
14	VDD	Supply	Positive supply voltage

Timing Waveforms

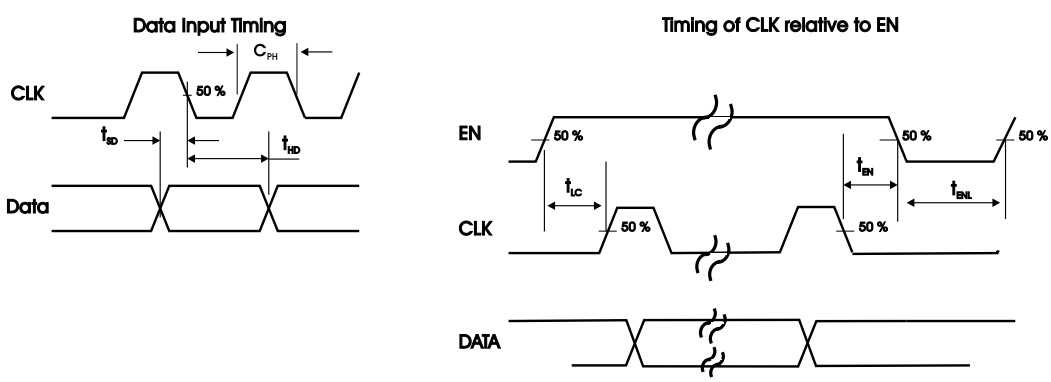


Figure 1: Detailed timing of serial interface

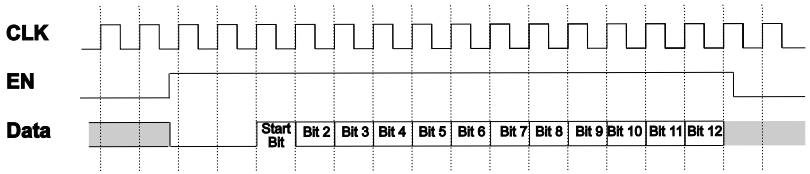


Figure 2: Serial write in double buffered mode. Registers are latched on falling edge of EN. Preceding ZEROs on DATA are ignored.

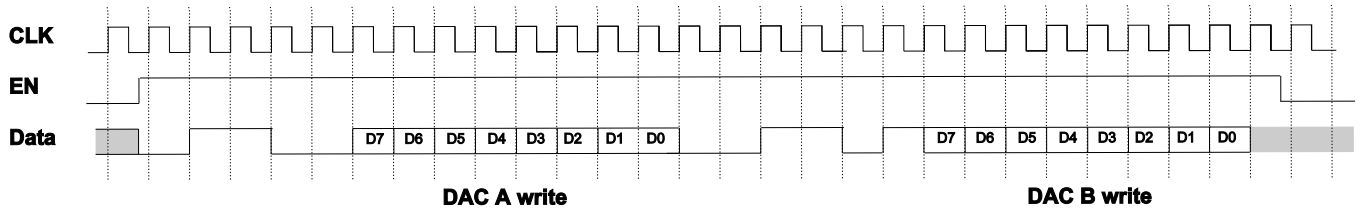


Figure 3: Multiple DAC updates at the same time are possible by holding EN high over multiple serial words. All DACs are updated on the falling edge of EN.

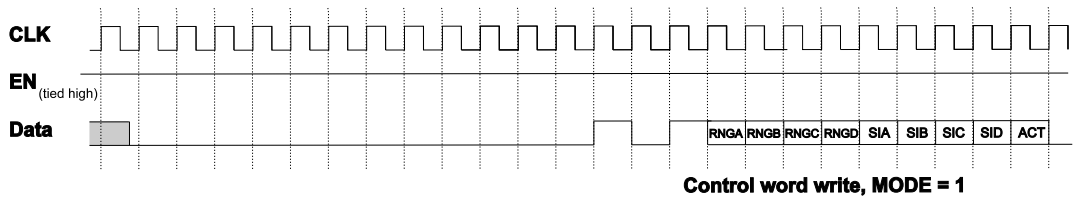


Figure 4: In single buffered mode, synchronisation can be regained by clocking in at least 12 ZEROs. Registers are updated on the twelfth falling edge of CLK after a Start Bit has been detected.

Functional Description

DAC operation

Each of WM5621L's four digital to analogue converters (DACs) are implemented using a single resistor string with 256 taps corresponding to each of the input 8-bit codes. One end of a resistor string is connected to the GND pin and the other end is driven from the output of a reference input buffer. The use of a resistor string guarantees monotonicity of the DAC's output voltage. Linearity depends upon the matching of the resistor string's individual elements and the performance of the output buffer. The reference input buffers present a high impedance to reference sources.

Each DAC has a voltage output amplifier which is programmable for gains of x1 or x2 through the serial interface. The DAC output amplifiers feature rail to rail output stages, allowing outputs over the full supply voltage range to be achieved with a x2 gain setting and a VDD/2 reference voltage input. Used in this way a slight degradation in linearity will occur as the output voltage approaches VDD.

Control of the WM5621L is effected through a serial interface using three dedicated pins, CLK, DATA and EN. A fourth pin (HWACT) is used to control the power-down controls to each of the 4 DACs.

Serial Interface

The serial interface uses the CLK pin to clock in data words presented serially on the DATA pin. The data words are 12 bits long and are written to either a control register or to one of the four DAC registers. When the EN pin is held low the serial interface is held in reset.

Figure 1 shows the format of the 12-bit data word transfer into the WM5621L. DATA is clocked on the falling edge of CLK. Every data word must start with a high start bit (preceeding zeros are ignored). The second bit is the register select bit which selects a write into either the control register or one of the DAC registers. Table 1 shows all valid write sequences.

The serial interface can operate in one of two ways, controlled by the setting of the MODE bit in the control register. The MODE bit defaults to 0 on power up which sets the device to work in a double buffered mode. When MODE is set to 1, the device operates in a single buffered mode, which can be controlled through only two pins (DATA and CLK, EN held high).

Double Buffered Mode

In normal operation the EN signal is used to control the latching of data. All DAC registers and all bits of the control word (other than MODE) are double buffered, with the second buffer only being enabled when the EN pin is taken low. In this way it is possible to update any number of DAC inputs at once by writing a 12-bit word to update each DAC register, with EN held high for all writes. When EN is pulled low at the end of the last write, all DAC inputs are latched at the same time. Figure 3 shows DACs A and B being written to in this way.

This mode also allows multiple devices to be share DATA and CLK lines by having only separate EN lines.

Single Buffered Mode

If the device is to be operated in single buffered mode, the EN pin should be tied high, and the interface is always active. The first write to the device after power-on should be a write to the control register to set the MODE bit high. The double buffered action is not possible as all words are latched across on the twelfth falling edge of CLK.

Loss of synchronisation may occur if glitches are present on the CLK and DATA inputs, a condition which may occur at power-on. If this has happened it is possible to regain synchronisation by clocking in at least 12 zeros (see Figure 4).

It is not possible to reset the MODE bit from 1 to 0. Operation of the device after any attempt to do this is undefined.

DAC Registers

Each DAC register holds an 8-bit unsigned byte to represent the DAC code. Table 1 indicates how these bytes are clocked into the DAC registers, with D7 being the most significant bit of the byte. These registers are reset to 0 at power-on.

Functional Description (continued)

Bit	Control Word	DACA Write	DACB Write	DACC Write	DACD Write
Start Bit Register Select	1 0	1 1	1 1	1 1	1 1
3	MODE	0	0	1	1
4	RNGA	0	1	0	1
5	RNGB	D7	D7	D7	D7
6	RNGC	D6	D6	D6	D6
7	RNGD	D5	D5	D5	D5
8	SIA	D4	D4	D4	D4
9	SIB	D3	D3	D3	D3
10	SIC	D2	D2	D2	D2
11	SID	D1	D1	D1	D1
12	ACT	D0	D0	D0	D0

Table 1

Bit	Power-up state	Function
MODE	0	Control serial interface
RNG A	1	DACA range select (0 = x1, 1 = x2)
RNG B	1	DACB range select (0 = x1, 1 = x2)
RNG C	1	DACC range select (0 = x1, 1 = x2)
RNG D	1	DACD range select (0 = x1, 1 = x2)
SIA	0	DACA shutdown inhibit
SIB	0	DACB shutdown inhibit
SIC	0	DACC shutdown inhibit
SID	0	DACD shutdown inhibit
ACT	0	Software shutdown control

Table 2

SIA	ACT	HWACT	DAC status
0	0	0	shutdown
0	0	1	shutdown
0	1	0	shutdown
0	1	1	active
1	0	0	active
1	0	1	active
1	1	0	active
1	1	1	active

Table 3

Control Register

The control register contains 10 active bits. The MODE bit controls the operation of the serial interface as described above. The function of the control register bits, and their state on power-up, are shown in table 2.

The shutdown state of each DAC is controlled through the shutdown inhibit bit for that channel (SIx), the ACT bit of the control register, and the HWACT pin. Table 3 shows the logical action of these three controlling bits for DAC A. It is possible, for example, to have any combination of DACs switched from shutdown to active by the HWACT pin, while the remaining DACs are held always active (achieve this by setting ACT=1, SIx=0 for the switching DACs, and SIx=1 for the always active DACs).

Linearity, offset, and gain error using single end supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier, with a negative voltage offset, attempts to drive the output to a negative voltage. However, because the most negative supply rail is GND, the output cannot drive to a negative voltage.

So when the output offset voltage is negative, the output voltage remains at ZERO volts until the input code value produces a sufficient output voltage to overcome the inherent negative offset voltage, resulting in the transfer function shown in Figure 5.

This negative offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive to a negative voltage.

Functional Description (continued)

For a DAC, linearity is measured between ZERO input code (all inputs 0) and full scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the break-point in the transfer function. So the linearity in the unipolar mode is measured between full scale code and the lowest code which produces a positive output voltage. The code is calculated from the maximum specification for the negative offset.

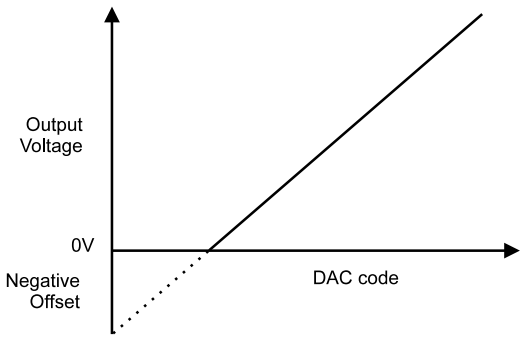
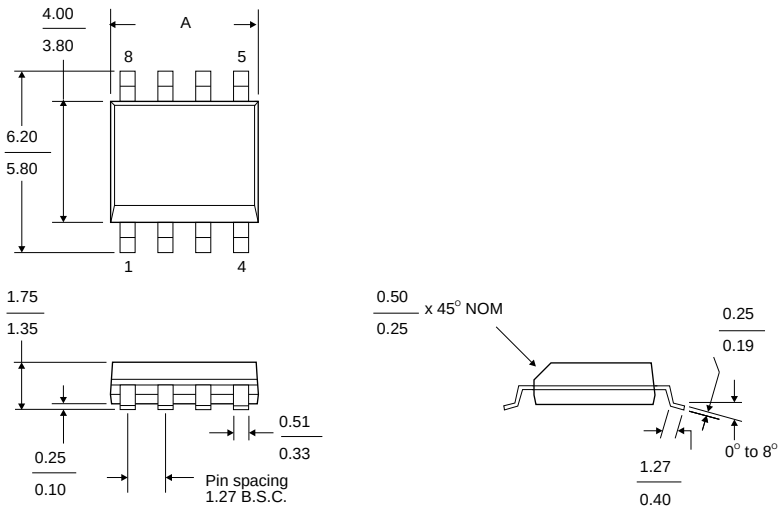


Figure 5: Effect of negative offset (single supply)

Package Descriptions

Plastic Small-Outline Package

D - 8 pins shown



Dimension 'A' Variations

N	Min	Max
8	4.80	5.00
14	8.55	8.75
16	9.80	10.00

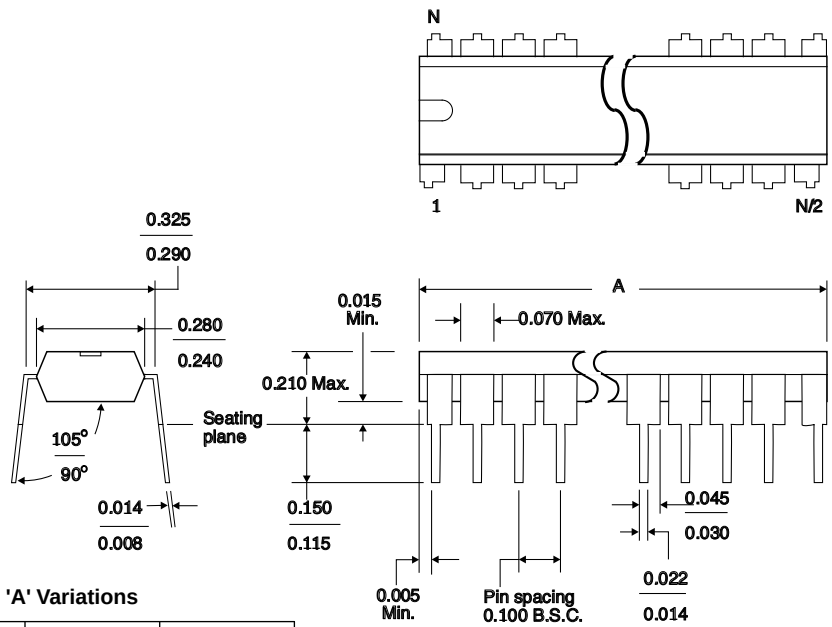
Notes:

A. Dimensions in millimeters.
B. Complies with Jedec standard MS-012.
C. This drawing is subject to change without notice.
D. Body dimensions do not include mold flash or protrusion.
E. Dimension A, mould flash or protrusion shall not exceed 0.15mm. Body width, interlead flash or protrusions shall not exceed 0.25mm.

Package Descriptions

Dual-In-Line Package

N or P



Dimension 'A' Variations

N	Min	Max
8	0.355	0.400
14	0.735	0.775
16	0.735	0.775
20	0.940	0.975

Notes:

A. Dimensions are in inches
B. Falls within JEDEC MS-001(20 pin package is shorter than MS-001)
C. N is the maximum number of terminals
D. All end pins are partial width pins as shown, except the 14 pin package which is full width.